06-20-00

Case Docket No. 00-415

THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Se Jeong Park et al.

FOR: **CACHE MEMORY FOR TEXTURE MAPPING PROCESS IN THREE-DIMENSIONAL GRAPHICS AND METHOD FOR REDUCING PENALTY DUE TO CACHE MISS**

Enclosed are:

(XXXXX) Five (5) sheets of drawings.

(XXXXX) An Assignment of the invention to Korea Advanced Institute of Science and Technology.

(XXXXX) A certified copy of Korean Application No. 99-23092, Filed June 19, 1999.

(XXXXX) Verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.

(XXXXX) Preliminary Amendment; Information Disclosure Statement.

The filing fee has been calculated as shown below:

For	No. Filed	No. Extra	SMALL ENTITY Rate	SMALL ENTITY Fee	OTHER THAN A SMALL ENTITY Rate	OTHER THAN A SMALL ENTITY Fee
Basic Fee				$ 345		$ 690
Total Claims	6	-20 =	x 9	$	x 18	$
Indep Claims	2	-3 = 0	x 39	$	x 78	$
Multiple Dependent Claim ( ) Presented			+130	$	+260	$
			TOTAL	$ 345	TOTAL	$

( ) Please charge my Deposit Account No. 02-0184 in the amount of $_____. A duplicate copy of this sheet is enclosed.

(XX) A check in the amount of $385.00 to cover the filing fee is enclosed.

(XX) The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 02-0184. A duplicate copy of this sheet is enclosed.

(X) Any additional filing fees required under 37 CFR 1.16.
(X) Any patent application processing fees under 37 CFR 1.17.

(XX) The Commissioner of hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 02-0184. A duplicate copy of this sheet is enclosed.

(X) Any patent application processing fees under 37 CFR 1.17.
(X) Any filing fees under 37 ~~CFR 1.16~~ for presentation of extra claims.

Date: June 19, 2000

Gregory P. LaPointe
Attorney for Applicants
Bachman & LaPointe, P.C.
Suite 1201-900 Chapel Street
New Haven, CT 06510-2802
Telephone: (203) 777-6628

Express Mail No. EL398545351US

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on June 19, 2000
(Date of Deposit)
Rachel Piscitelli
Name and Reg. No. of Attorney
Rachel Piscitelli
Signature
June 19 2000
Date of Signature

PATENT

Attorney's Docket No. 00-415

Applicant or Patentee: Se-Jeong Park et al.

Serial or Patent No.: 0 /

Filed or Issued:

For: CACHE MEMORY FOR TEXTURE MAPPING PROCESS IN THREE DIMENSIONAL GRAPHICS AND MEMORY FOR REDUCING PENALTY DUE TO CAHCE MISS

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9 (f) and 1.27(d))—NONPROFIT ORGANIZATION

I hereby declare that I am an official empowered to act on behalf of the nonprofit organization identified below:

NAME OF ORGANIZATION Korea Advanced Institute of Science and Technology

ADDRESS OF ORGANIZATION 373-1 Kusong-dong, Yusong-ku, 305-701, Taejon-si, Republic of Korea

TYPE OF ORGANIZATION

- [X] UNIVERSITY OR OTHER INSTITUTION OF HIGHER EDUCATION
- [ ] TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501 (a) and 501 (c)(3))
- [ ] NONPROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA
  (NAME OF STATE _____)
  (CITATION OF STATUTE _____)
- [ ] WOULD QUALIFY AS TAX EXEMPT UNDER INTERNAL REVENUE SERVICE CODE (26 USC 501 (a) and 501 (c)(3)) IF LOCATED IN THE UNITED STATES OF AMERICA
- [ ] WOULD QUALIFY AS NONPROFIT SCIENTIFIC OR EDUCATIONAL UNDER STATUTE OF STATE OF THE UNITED STATES OF AMERICA IF LOCATED IN THE UNITED STATES OF AMERICA
  (NAME OF STATE _____)
  (CITATION OF STATUTE _____)

I hereby declare that the nonprofit organization identified above qualifies as a nonprofit organization as defined in 37 CFR 1.9(e) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code with regard to the invention entitled

by inventor(s) Se Jeong Park, Hoi Jun Yoo, and Kyu Ho Park

described in

- [X] the specification filed herewith.
- [ ] application serial no. 0 / _____ , filed _____ .
- [ ] patent no. _____ , issued _____ .

I hereby declare that rights under contract or law have been conveyed to and remain with the nonprofit organization with regard to the above identified invention.

If the rights held by the nonprofit organization are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

*NOTE: *Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27).*

NAME _____

ADDRESS _____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME _____

ADDRESS _____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any charge in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Duk-In CHOI

TITLE IN ORGANIZATION Korea Advanced Institute of Science and Technology

ADDRESS OF PERSON SIGNING 373-1 Kusong-dong, Yusong-ku, 305-701, Taejon-si, Republic of Korea

SIGNATURE Choi Duk-In Date Apr. 29. 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Se Jeong Park et al. Docket No.: 00-415

Serial No.: Examiner :

Filed : Art Unit :

For : CACHE MEMORY FOR TEXTURE MAPPING PROCESS IN THREE -DIMENSIONAL GRAPHICS AND METHOD FOR REDUCING PENALTY DUE TO CACHE MISS

Suite 1201
900 Chapel Street
New Haven, CT 06510-2802

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents & Trademarks
United States Patent & Trademark Office
Washington, D.C. 20231

Dear Sir:

In the above-identified application for United States patent, please amend as follows.

IN THE CLAIMS

Please amend the following claim.

Claim 5, lines 1 and 2, delete "any one of Claims 1 to 4," and insert therefor --Claim 1,--.

REMARKS

Amendments have been made to the claims to remove the multiple dependencies in order to conform with U.S. practice. An early action on the merits is respectfully requested.

If any fees are required in connection with this case, it is respectfully requested that they be charged to Deposit Account No. 02-0184.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

June 19, 2000
(Date of Deposit)

Rachel Piscitelli
Name and Reg. No. of Attorney

Signature

June 19, 2000
Date of Signature

Respectfully submitted,

Se Jeong Park et al.

By

Gregory P. LaPointe
Attorney for Applicants
Telephone - (203) 777-6628

Date: June 19, 2000

Express Mail No.
EL398545351US

CACHE MEMORY FOR TEXTURE MAPPING PROCESS IN THREE-DIMENSIONAL GRAPHICS AND METHOD FOR REDUCING PENALTY DUE TO CACHE MISS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a cache memory for a texture mapping process which is applicable to a high performance three-dimensional graphics card for a personal computer, three-dimensional game machines and other fields requiring small and high performance three-dimensional graphics. More particularly, the present invention relates to a cache memory capable of accelerating a texture mapping process based upon a hardware-used mipmapping process using a trilinear interpolation, and a method enabling a reduction in penalty due to a cache miss by, with hardware-based prediction, prefetching textures to be needed in the future.

Description of the Prior Art

For a three-dimensional graphics system, a texture mapping technique is mainly used to obtain more realistic scenes. Texture mapping is a technique that applies a

two-dimensional image acquired by a camera, onto an object's surface in order to have a textured surface of a three-dimensional object, wherein the texture refers to a two-dimensional source image and each point element in the texture is called a texel to be associated with each pixel of the displayed portion.

Rather than, after applying the two-dimensional image, or texture, on a surface of the three-dimensional object, projecting the result to a two-dimensional display screen, a method permitting a reduction in computational amount in applying the above-mentioned texture mapping technique is used which includes obtaining coordinates of the object's surface in the three-dimensional space from each pixel of the image projected to the two-dimensional screen, computing two-dimensional texture coordinates corresponding thereto to obtain associated texels, and defining colors of the pixels to be represented on the display screen.

However, such a texture mapping technique causes an aliasing phenomenon, because an area in the texture space, mapped to one pixel represented on the display screen, is not exactly mapped to an area of one texel.

The concept of the mipmapping technique will be explained with reference to Fig. 1 representing an example. On the right side of Fig. 1, there is shown a road

projected to the two-dimensional display screen. Assuming that pixels located near the observer and associated with an area 'a' or 'b' of the projected road are to be mapped into one texel in the texture space, other pixels located far from the observer and associated with, such as, an area 'c' or 'd' would be mapped into the texels in the texture space. Therefore, one texture, capable of being representative of the texels, needs to be taken to be mapped into one pixel on the display screen. Otherwise, a distorted image results.

As an easy method of obtaining one representative texel, a method is frequently used in which the representative texel is obtained by taking an average of the values of all texels in the area mapped into the texture space, which method is called a texture filtering.

However, since the above-described texture filtering is a time consuming process, the mipmapping technique is frequently used as a less time consuming process.

In the mipmapping process, as shown on the left side of Fig. 1, the original or base texture image (which is an image indicated by LOD 0 in Fig. 1, wherein the LOD (Level Of Detail) denotes a value representing the number of texels to which one pixel on the display screen corresponds) is pre-filtered and subsampled to prepare

textures or mipmaps of various LOD levels. Based upon the LOD and (u, v) coordinates which are computed at the time when the pixel to be displayed on the screen is mapped into the texture space, the texels required are taken from appropriate LOD levels on the mipmap and then displayed on the screen.

While the computed LOD value and (u, v) coordinates which are mapped onto the texture space appear as mixed numbers, respectively, i.e., (x, y) coordinates on the screen in integer representation are coordinate-transformed by using a transform matrix to give the mixed numbers, the values presently existing on the mipmap are associated with the locations of the integer value of the LOD and the (u, v) coordinates in integer representation. Accordingly, there is no texel value at the location of the precise LOD and (u, v) coordinates in the texture space into which the pixel to be rendered on the display screen is mapped. However, the integer values nearest those non-integer texel values are read from the mipmap, and then the distance difference between the read values and the values at the accurate locations are used for the interpolation.

Referring to Fig. 2, the following is to explain an example on how to obtain the texel value with respect to a pixel mapped with the LOD=0.6 and (u, v)=(23.25, 30.50).

(i) Since the value of the LOD is 0.6, the (23, 30), (23, 31), (24, 30) and (24, 31) coordinates are selected from integers that are nearest to the values of u=23.25 and v=30.50, at the level of LOD 0, from which the texel values are read to obtain the representative value at the level of LOD 0, based on the distance between the actual exact coordinates and those coordinates.

(ii) To obtain the representative value at the level of LOD 1, the (11, 15), (11, 16), (12, 15) and (12, 16) coordinates are selected from integers that are nearest to the values of u=23.25/2=11.62 and v=30.50/2=15.25, from which the telex values are read to obtain the representative value at the level of LOD 1, based on the distance between the actual exact coordinates and those coordinates.

(iii) The difference between the two representative values thus obtained and the actual exact value, 0.6 of LOD, is used to obtain the final representative texel value, as shown in Fig. 2.

The mipmapping technique previously prepares the textures with various levels of the LOD for high-speed texture mapping, reads eight texels to obtain a representative texel value to be used in executing the program, and performs the interpolation (such an

interpolation method is called a trilinear interpolation) and uses the interpolated resulting value as a representative value.

While the above-mentioned mipmapping technique provides more rapid processing, a problem still remains in that a large amount of time is required to sequentially read eight texels from the memory which is needed to perform the three-dimensional graphics mipmapping process.

Therefore, in order to solve such a problem, there has been proposed a structure as shown in Fig. 3, which enables a representative texel value to be obtained, by providing separate memory banks capable of storing texels of two levels of LOD, accessing simultaneously eight texels using the memory banks where the texels are stored with the mapping relation between the texels stored in each of the memory banks and the position of the texels in the texture space, as shown in Fig. 4 (where a number in each texel area denotes a memory bank number to which the texel is to be stored) and sending the accessed eight texels to the trilinear interpolator to perform the interpolation in one clock cycle, and obtaining a representative texel value.

However, since various sizes of texture images are used in applications of the actual three-dimensional graphics system, the use of texram as shown in Fig. 3 leads

to the need of a memory of more capacity than that of a texture image to be used in the future. In a case where the value of the LOD greatly varies every time each pixel is rendered, the time is considerably consumed in a continuous change of the contents of the memory. This results in inefficient use of the memory and an increase in cost. Thus, the structure as shown in Fig. 3 has a drawback in the practical use.

Proposed as another common concept is a clipmap, which enables a great reduction in the memory capacity of the system in a texture mapping process using a large texture image. In this scheme, since on the mipmap as shown in Fig. 5, the lower the LOD level is, the more the space for storing the texture image is increased in geometrical progression, only the textures of several upper levels of the LOD are placed in upper portions of the current system memory, and the currently rendered portions among the reaming values of the LOD levels are also placed. If necessary, other portions can be fetched and used from a hard disk where the overall mipmap has been stored.

However, the above-mentioned clipmap method is applied between the hard disk and the system memory and entirely implemented in a software manner. Therefore, the main object of this method is essentially to reduce the capacity

of the system memory, but not suitable for accelerating the texture mapping.

SUMMARY OF THE INVENTION

An object of the present invention is to solve the problems of a conventional prior art, and to provide a cache memory capable of accelerating a hardware-based mipmapping process, while a concept of a clipmap is applied to the relation between a system memory and a cache memory for a texture mapping process, and a method for reducing a penalty due to a cache miss.

The concept in technology for achieving the above-mentioned objects resides in a cache having a special structure making it possible that a cache memory for storing only textures by a working set in a moderate size thereof is prepared, all eight texels needed to perform a trilinear interpolation only in one clock cycle are accessed to obtain a final texel value, whereby various sizes of texture images are effectively processed and texture mapping acceleration becomes possible even for small and low cost systems.

The reduction of a penalty occurring at the time when a cache miss occurs can be accomplished by prefetching the

textures to be needed in the future, by virtue of a hardware implemented for the prediction.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a conceptional diagram of a mipmapping process;

Fig. 2 is a diagram for explaining an example of a trilinear interpolation;

Fig. 3 is a diagram showing a structure of a texram;

Fig. 4 is a diagram showing an arrangement of texels in the texram;

Fig. 5 is a conceptional diagram of a clipmap;

Fig. 6 is a conceptional diagram for explaining a cache memory for a texture mapping process according to one embodiment of the present invention;

Fig. 7 is a diagram for showing a structure of a cache memory for a texture mapping process according to one embodiment of the present invention;

Fig. 8 is a diagram for showing procedures of

predicting and replacing texture sub-clips; and

Fig. 9 is a diagram for showing procedures of predicting and replacing a texture stack layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The concept of a cache memory used in a texture mapping process is shown in Fig. 6, wherein the cache memory consists of a clip RAM pyramid in which all texels of several upper levels (e.g., five levels) of LOD are stored and a clip RAM stack in which only a working set currently needed among the remaining LOD levels is stored.

The clip RAM stack is able to store therein the working set of four levels of LOD, each level consisting of sixteen (4 by 4) sub-clips. These sub-clips may be, even at a normal operation, as well as at cache miss occurrence, replaced with the contents from an external memory which stores the whole mipmap, by a sub-clip predictor for predicting the required sub-clips in advance. Thus, the prefetch by the hardware is made possible, which leads to the reduction of the cache miss penalty.

The cache memory organization for the texture mapping according to the above-mentioned concept is shown in Fig. 7.

The cache memory may be organized to include a first DRAM bank 10 configured as a clip RAM pyramid for storing all texels associated with several upper levels (e.g., five levels) of LOD, and a second DRAM bank 20 configured as a clip RAM stack for storing only a working set currently needed among the remaining levels of LOD, wherein both first and second DRAM banks 10 and 20 have respective SAM (Serial Access Memory) ports used for reading the texture for trilinear interpolation and bringing new texture sub-clips from the outside. The cache memory also includes a sub-clip loader 30 connected to the SAM ports of the first and second DRAM banks 10 and 20, and for fetching new texture sub-clips from an external memory, a trilinear interpolator 40 for taking four texels from respective two layers on the mipmap and performing the trilinear interpolation, a sub-clip predictor 50 for performing a hardware-based prediction and prefetching the sub-clips in order to reduce a penalty due to cache miss, a controller 60 for controlling the above components, and a CAM (Content Addressable Memory) 21 for checking if eight texels existing at an integer coordinate relative to an LOD and (u, v) coordinates are located in the first and second DRAM banks 10 and 20, when the LOD and (u, v) coordinates mapped into a texture space with respect to a pixel to be rendered

on a display screen are input to the controller 60.

The basic operation of the cache memory for the texture mapping thus structured will be explained.

All texels for a current texture, also associated with several upper levels of LOD, are stored in the first DRAM bank 10 for the clip RAM pyramid, whose contents, therefore, do not need to be changed during the processing. Since the second DRAM bank 20 for the clip RAM stack stores, however, only the working set currently needed, the continuous change of the contents thereof is required. In case the LOD and (u, v) coordinates in the texture space into which a pixel to be presently drawn is mapped are entered, the CAM (Content Addressable Memory) 21 is used to check the first and second DRAM banks 10 and 20 as to if eight texels exist at the coordinates on the integer basis, with respect to the LOD and (u, v) coordinates or not, and if found, the found eight texels are simultaneously read to subsequently perform the trilinear interpolation in the trilinear interpolator 40.

However, if not found, the cache miss occurs. At this time, the controller 60 makes the sub-clip loader 30 take from the external memory the sub-clips containing the necessary texels which are read by the trilinear interpolator 40 performing the trilinear interpolation.

To reduce a penalty in the event of the cache miss, the cache memory for the texture mapping according to the present invention is provided with the sub-clip predicator 50 which predicts the sub-clips to be soon needed, whereby it is possible to load from the outside new sub-clips not colliding with the sub-clips now being accessed during the normal texture cache operation.

The function of predicting the sub-clips, which the cache memory for the texture mapping has according to one embodiment of the present invention, will be explained in detail. It is possible to prefetch the contents of the cache memory on a sub-clip basis when the hardware-based prediction is made which includes two predictions, i.e., sub-clip prediction in one stack layer and stack layer prediction.

The prediction on the sub-clip in one stack layer will be explained.

Fig. 8 shows procedures on how to predict and replace the sub-clip to be soon needed, in which an upper left drawing in Fig. 8 illustrates an image on a two-dimensional display screen when, for example, a street in three dimensions is projected to the two-dimensional display screen. Typically, an object in the three-dimensional space may be represented as small triangles, which are

stored in a data file as a set in which a series of triangles are collected. Therefore, when the street is rendered on the display screen as in Fig. 3, a series of triangles are in order rendered in a direction indicated by an arrow.

Referring to a lower left drawing in Fig. 8, four vertexes a, b, c and d of the texture image to be applied to the street are mapped into four vertexes a, b, c and d of the street shown in the upper left drawing in Fig. 8. A series of triangles on the display screen will be in order drawn in a direction indicated by an arrow. The access pattern of the texture image necessary for rendering has a feature in that the access is conducted in a direction indicated by an arrow represented in a left lower drawing in Fig. 8.

The use of such a feature may result as in the drawing to the right in Fig. 8 showing that the sub-clips on specific stack layers are predicted and replaced. The 4 by 4 sub-clips (current clips), represented as the shaded portions in the drawing, are the sub-clips in the current clip RAM stack. The trace on the (u, v) coordinates is shown as one example in which the texels are accessed over time. As shown in the drawing, the sub-clips may be bounded by the 2 x 2 sub-clips in size due to the

hardware-based prediction limitation. If the tracing of the (u, v) coordinates goes beyond the boundary, the sub-clips to be soon needed will be prefetched to reduce the penalty at the time of the cache miss being likely to occur lately, even if the cache miss at this stage does not occur. The drawing shows the case of the tracing of the (u, v) coordinates which deviates from the prediction limitation. In this case, four sub-clips on the portions lightly shaded are prefetched and put into a left side area of 4 by 4 sub-clips. The prefetching is thus made possible based on the hardware-based prediction using the texture access scheme, and at the best case, it is possible to make the required sub-clips exist in the cache memory for the texture mapping, without the cache miss occurrence.

Fig. 9 shows procedures on how to predict and replace the stack layer needed depending upon the change of the LOD, in which both left upper and lower drawings in Fig. 9 are identical with those in Fig. 8. As shown in the drawing, when a series of triangles are rendered in a direction indicated by an arrow, a continuously increasing change of the LOD is generally observed, even if there is a minute change of the LOD. A right side drawing in Fig. 9 shows the tracing of the LOD which continuously increases. The current clip RAM stacks represent the

levels of the LOD stored in the current clip RAM stack, among which two levels of the LOD are used as the prediction limitation on the stack layer. In this example, immediately after the tracing of the LOD reaches the LOD i+2, the contents of the stack layer corresponding to the LOD i+4 are loaded into an area having stored the contents of the LOD i, which means that the stack layer can also be, as with the sub-clips, prefetched based upon the hardware-based prediction.

As described above, the cache memory for the three-dimensional graphics texture mapping makes possible the hardware-based accelerated mipmapping process using the trilinear interpolation for various texture images in sizes thereof, and can also be applied to a small and low cost three-dimensional graphics system, whereby it is possible to provide a more realistic high-speed three-dimensional graphics process.

Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

WHAT IS CLAIMED IS:

1. A cache memory for three-dimensional graphics texture mapping, comprising:

first and second DRAM banks including SAM ports, respectively, each of said SRAM ports reading a texture for a trilinear interpolation and fetching new texture sub-clips from the outside;

a sub-clip loader connected to said SAM ports of said first and second DRAM banks and for fetching new texture sub-clips from an external memory;

a controller for controlling said components; and

a CAM for checking if eight texels existing at an integer coordinate relative to an LOD and (u, v) coordinates are located in said first and second DRAM banks, when the LOD and (u, v) coordinates mapped into a texture space with respect to a pixel to be rendered on a display screen are input to said controller.

2. The cache memory according to Claim 1, wherein said first DRAM bank forms a clip RAM pyramid for storing all texels associated with several upper levels of the LOD among overall mipmaps, and wherein said second DRAM bank forms a clip RAM stack for storing only a working set

currently needed among the remaining LOD levels being not stored in said first DRAM bank.

3. The cache memory according to Claim 1, wherein said second DRAM bank has a plurality of n x n sub-clips obtained by dividing a texture area on one level of LOD of the mipmap, and the contents of said cache memory are replaced on the sub-clip basis.

4. The cache memory according to Claim 1, wherein data paths are provided between said first and second DRAM banks and a trilinear interpolator, said data paths being adapted to access eight texels existing at the integer coordinate locations centered on (u, v) coordinates and LOD mapped into a texture space of a pixel to be rendered on a display screen, such that a trilinear interpolation is performed in one clock cycle.

5. The cache memory according to any one of Claims 1 to 4, further comprising a sub-clip predictor for performing a hardware-based prefetch of a sub-clip to be soon needed, so as to reduce a penalty due to cache miss.

6. A method for reducing a penalty occurring upon a

cache miss, comprising the steps of:

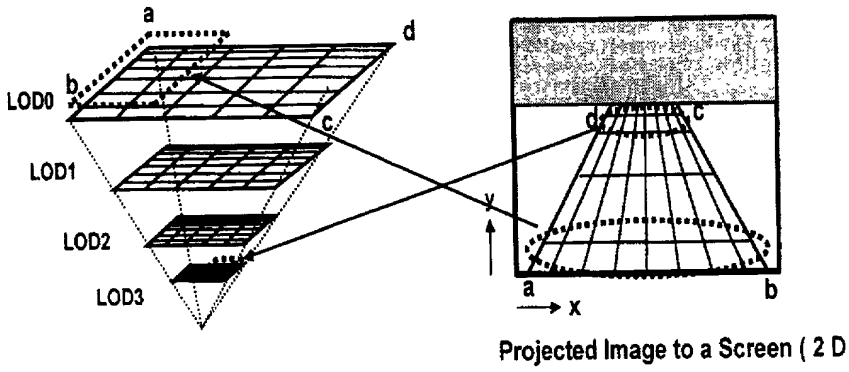
performing a sub-clip prediction in one stack layer, where, under a hardware-based sub-clip prediction limit of 2 by 2 sub-clip boundary inside of sub-clips (4 by 4) on a current clip RAM stack, when the tracing of (u, v) coordinates passes the limit, sub-clips of the tracing direction (left, right, upper and lower sides) are prefetched; and

performing a stack layer prediction where the current clip RAM stack represents the levels of LOD (LOD i to LOD i+3) stored in said stack, internal two levels of LOD are used as a prediction limit, and, immediately after the tracing of LOD passes the limit, a stack layer corresponding to a next level of LOD is prefetched.

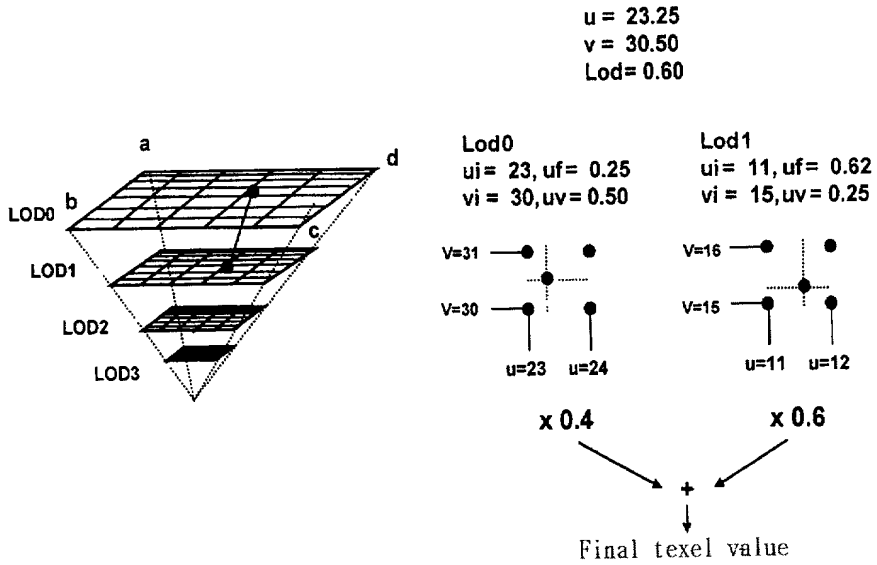
ABSTRACT OF THE DISCLOSURE

A cache memory for a texture mapping process which is applicable to a high performance three-dimensional graphics card for a personal computer, three-dimensional game machines and other fields requiring small and high performance three-dimensional graphics. In particular, in order to accelerate a texture mapping process based upon a hardware-used mipmapping process using a trilinear interpolation in a three-dimensional graphics system, there is provided a cache memory in which only textures by a moderate size of a working set are stored, and all eight texels needed to perform a trilinear interpolation only in one clock cycle are accessed to obtain a final texel value, and a method enabling a reduction in penalty due to a cache miss by, with hardware-based prediction, prefetching textures to be needed in the future. The invention makes it possible that various sizes of texture images are effectively processed and texture mapping acceleration becomes possible even for small and low cost systems, as compared with a conventional hardware-based texture mapping acceleration method.

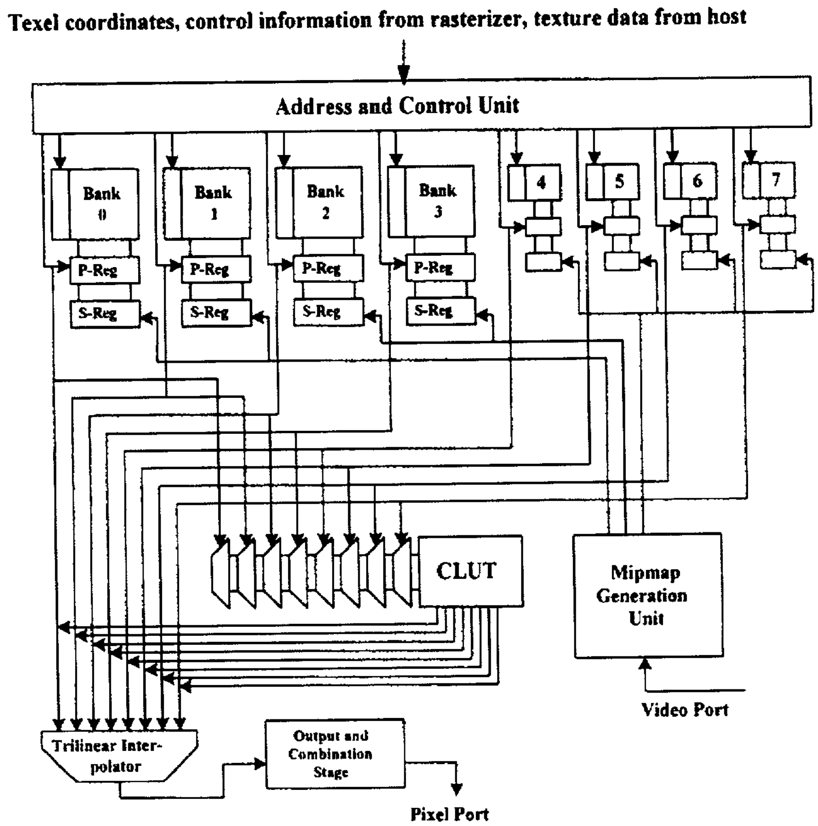
【Fig 1】


a
d
b
LOD0
c
LOD1
LOD2
LOD3
y
d
c
a
x
b
Projected Image to a Screen (2 D

【Fig 2】


u = 23.25
v = 30.50
Lod= 0.60
a
d
b
LOD0
c
LOD1
LOD2
LOD3
Lod0
ui= 23, uf= 0.25
vi = 30, uv= 0.50
Lod1
ui= 11, uf= 0.62
vi = 15, uv= 0.25
V=31
V=30
u=23
u=24
V=16
V=15
u=11
u=12
x 0.4
x 0.6
+
Final texel value

【Fig 3】



【Fig 4】

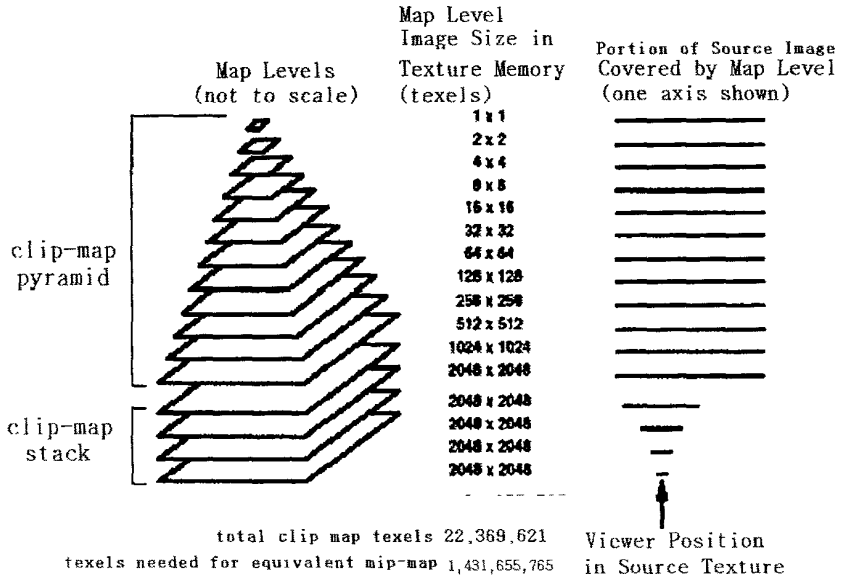
0	1	0	1	0	1	0	1	0	1	0	1
2	3	2	3	2	3	2	3	2	3	2	3
0	1	0	1	0	1	0	1	0	1	0	1
2	3	2	3	2	3	2	3	2	3	2	3
0	1	0	1	0	1	0	1	0	1	0	1
2	3	2	3	2	3	2	3	2	3	2	3
0	1	0	1	0	1	0	1	0	1	0	1
2	3	2	3	2	3	2	3	2	3	2	3
0	1	0	1	0	1	0	1	0	1	0	1
2	3	2	3	2	3	2	3	2	3	2	3
0	1	0	1	0	1	0	1	0	1	0	1
2	3	2	3	2	3	2	3	2	3	2	3

(LOD i)

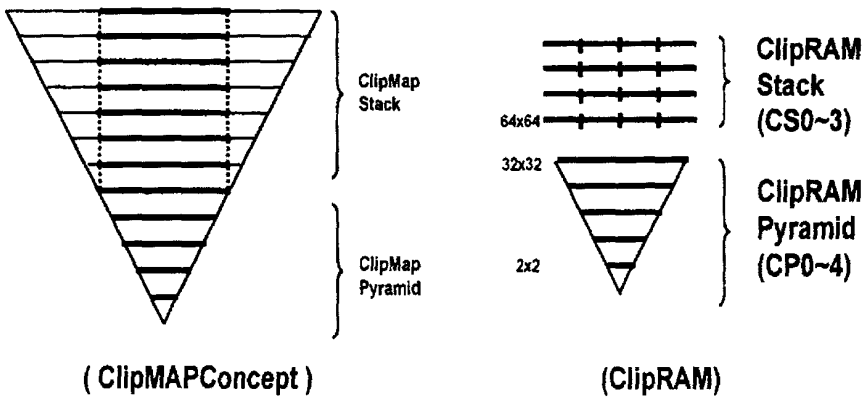
4	5	4	5	4	5
6	7	6	7	6	7
4	5	4	5	4	5
6	7	6	7	6	7
4	5	4	5	4	5
6	7	6	7	6	7

(LOD i+1)

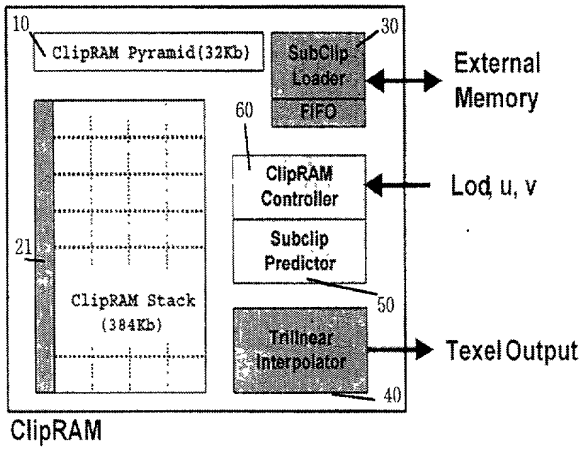
【Fig 5】


Map Levels
(not to scale)
Map Level
Image Size in
Texture Memory
(texels)
Portion of Source Image
Covered by Map Level
(one axis shown)
clip-map
pyramid
clip-map
stack
1 x 1
2 x 2
4 x 4
8 x 8
16 x 16
32 x 32
64 x 64
128 x 128
256 x 256
512 x 512
1024 x 1024
2048 x 2048
2048 x 2048
2048 x 2048
2048 x 2048
2048 x 2048
total clip map texels 22,369,621
texels needed for equivalent mip-map 1,431,655,765
Viewer Position
in Source Texture

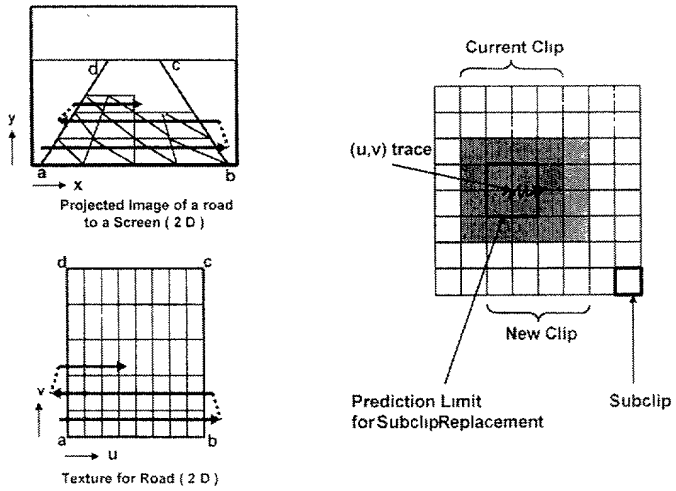
【Fig 6】


ClipMap
Stack
ClipMap
Pyramid
64x64
32x32
2x2
ClipRAM
Stack
(CS0~3)
ClipRAM
Pyramid
(CP0~4)
(ClipMAPConcept)
(ClipRAM)

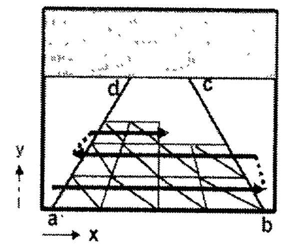
【Fig 7】


10
ClipRAM Pyramid(32Kb)
30
SubClip Loader
FIFO
External Memory
60
ClipRAM Controller
Lod, u, v
Subclip Predictor
21
ClipRAM Stack (384Kb)
50
Trilinear Interpolator
Texel Output
40
ClipRAM

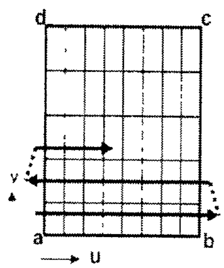
【Fig 8】


d
c
y
a
x
b
Projected Image of a road to a Screen (2 D)
d
c
v
a
b
u
Texture for Road (2 D)
Current Clip
(u,v) trace
New Clip
Prediction Limit for SubclipReplacement
Subclip

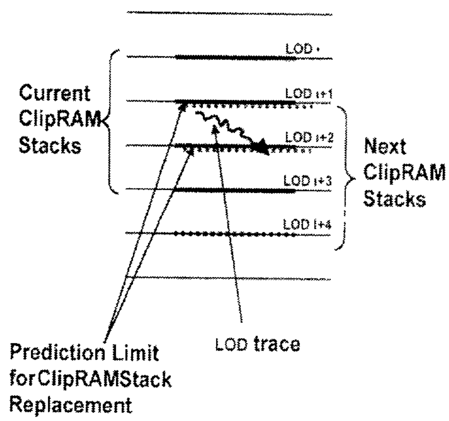
【Fig 9】



Projected Image of a road to a Screen (2 D)



Texture for Road (2 D)



PATENT

Attorney's Docket No. 00-415

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR CIP)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: *(check one applicable item below)*

- ☑ original
- ☐ design
- ☐ supplemental

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application, do not check next item; check appropriate one of last three items.

- ☐ national stage of PCT

NOTE: If one of the following 3 items apply, then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR CIP.

- ☐ divisional
- ☐ continuation
- ☐ continuation-in-part (CIP)

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims, an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

CACHE MEMORY FOR TEXTURE MAPPING PROCESS IN THREE-DIMENSIONAL GRAPHICS AND METHOD FOR REDUCING PENALTY DUE TO CACHE MISS

SPECIFICATION IDENTIFICATION

the specification of which: *(complete (a), (b) or (c))*

(a) ☑ is attached hereto.

(b) ☐ was filed on _____ as ☐ Serial No. 0 /_____ or ☐ Express Mail No., *as Serial No. not yet known* _____ and was amended on _____ *(if applicable)*.

NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) ☐ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____ *(if any)*.

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information

☒ which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56

(also check the following items, if desired)

☒ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent, and

☒ In compliance with this duty there is attached an information disclosure statement in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. § 119)

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) ☐ no such applications have been filed.

(e) ☑ such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. itself claimed priority check item (e), enter the details below and make the priority claim.

A. PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

COUNTRY (OR INDICATE IF PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
KR	99-23092	19. 06. 1999	☑ YES NO ☐
			☐ YES NO ☐
			☐ YES NO ☐
			☐ YES NO ☐
			☐ YES NO ☐

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

NOTE: *If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CIP APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.*

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*List name and registration number*)

Robert H. Bachman (19,374), Gregory P. LaPointe (28,395), Barry L. Kelmachter (29,999), and George A. Coury (34,309), all of Bachman & LaPointe, P.C., 900 Chapel Street, Suite 1201, New Haven, CT 06510-2802

(check the following item, if applicable)

☐ Attached as part of this declaration and power of attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO

Bachman & LaPointe, P.C.
900 Chapel Street, Suite 1201
New Haven, CT 06510-2802

DIRECT TELEPHONE CALLS TO:
(Name and telephone number)

Gregory P. LaPointe
(203) 777-6628

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE *Carefully indicate the family (or last) name as it should appear on the filing receipt and on other documents*

Full name of sole or first inventor

Se Jeong (GIVEN NAME) _____ (MIDDLE INITIAL OR NAME) PARK (FAMILY (OR LAST NAME))

Inventor's signature _____

Date June 7, 2000 Country of Citizenship KR

Residence Dept. of Electric and Electronics, KAIST, 373-1 Kusong-dong, Yusong-ku, 305-701, Taejon-si, Republic of Korea

Post Office Address same as above

Full name of second joint Inventor, if any

Hoi Jun (GIVEN NAME) _____ (MIDDLE INITIAL OR NAME) YOO (FAMILY (OR LAST NAME))

Inventor's signature _____

Date June 7, 2000 Country of Citizenship KR

Residence #103-705 Hyundai Apt. Doryong-song, Yusong-ku, 305-340, Taejon-si, Republic of Korea

Post Office Address same as above

Full name of third joint inventor, if any

Kyu Ho (GIVEN NAME) _____ (MIDDLE INITIAL OR NAME) PARK (FAMILY (OR LAST NAME))

Inventor's signature _____

Date June 7, 2000 Country of Citizenship KR

Residence #132-202 Hanbit Apt., Kusong-dong, Yusong-ku, 305-388, Taejon-si, Republic of Korea

Post Office Address same as above

Full name of 4th joint inventor, if any

_____ (GIVEN NAME) _____ (MIDDLE INITIAL OR NAME) _____ (FAMILY (OR LAST NAME))

Inventor's signature _____

Date _____ Country of Citizenship _____

Residence _____

Post Office Address _____

Full name of 5th joint inventor, if any

_____ (GIVEN NAME) _____ (MIDDLE INITIAL OR NAME) _____ (FAMILY (OR LAST NAME))

Inventor's signature _____

Date _____ Country of Citizenship _____

Residence _____

Post Office Address _____

CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGE(S) WHICH FORM A PART OF THIS DECLARATION

☐ Signature for sixth and subsequent joint inventors. *Number of pages added* _____

* * *

☐ Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _____.

* * *

☐ Signature for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. *Number of pages added* _____

* * *

☐ Added page for signature by one joint inventor on behalf of deceased inventor(s) where legal representative cannot be appointed in time (37 CFR 1.47).

* * *

☐ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (C-I-P) application.

☐ Number of pages added _____

* * *

☐ Authorization of attorney(s) to accept and follow instructions from representative.

* * *

(If no further pages form a part of this Declaration, then end this Declaration with this page and check the following item:)

☒ This declaration ends with this page.